TECHNICAL NOTE 2:

USE OF WOBBLE CLOCKING TO SUPPRESS DARK CURRENT

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1 The Eddington FT CCD

This document describes a series of dark current measurements performed on an E2V type CCD42-C0-2-C24 frame-transfer CCD. The device measures 2k×6k×13μm pixels. The image area is divided into two equal zones each containing 3k rows. The lower zone is over-coated with Aluminium so as to define a frame store and can be clocked independently to the upper zone. The serial register is also divided left-right so as to permit split frame readout through two amplifiers. Only the left hand side of the serial register could be made to work. The CCD was mounted in a cryostat and cooled with a Cryotiger close-cycle cooler. The temperature was accurately servoed using a Lakeshore controller. In its final application it is highly desirable to operate this CCD using a Peltier cooler so as to simplify the cryostat design. Since it will be used for rapid photometry with the exposure times < 30s, there is at least the possibility of the higher Peltier operating temperatures being acceptable. In this study the dark current as a function of operating temperature is investigated.

Additionally the use of 'wobble-clocking' or Dither (Jorden et al. [2]) is explored as a way of reducing the dark current.

2 Dark current measurement technique

The cryostat window was taped shut with a metallic lid. A 10 minute dark frame was taken to confirm that the dark current signal in the two image areas was the same. Since only one of these was sensitive to light, the other being covered with an Aluminium shield, any difference in signal in these two zones would indicate a light leak. The gain of the system in e^-/ADU was measured using the photon transfer technique. For this an LED mounted on the outside of the cryostat window was used as a light source. Dark current was measured using two small windows within the CCD image. One window lay in the first hundred rows of the frame store (the part overlaid with Aluminium). The second window that was used to measure the bias level was placed within the right hand part of the image corresponding to the non-functioning serial register. The dark current was therefore equal to the difference in the mean signal in these two windows multiplied by the system gain and divided by the exposure time. The measured dark currents were expressed in units of e^- $pixel^{-1}$ $hour^{-1}$. The readout time for the full CCD was 70s and the read noise was approximately $5e^-$ RMS.

3 Dark current versus temperature

The first series of measurements involved taking 30s dark currents at four temperatures. At each temperature setting at least an hour was allowed for stabilisation. During the integration of the dark frames only a single vertical phase was held high (+3V with respect to substrate). The other two phases were held constant at -9V with respect to the substrate i.e. in their inverted states. The results are shown in the red plot of Figure 1. This indicates that the dark current drops below $1e^-s^{-1}$ at a temperature of about 219K.

The E2V data sheet for the CCD4290 (a similar device to the Eddington CCDs) gives an equation describing the dark current as a function of temperature relative to the dark current at room temperature. Although the room temperature dark current was not measured, the following relation (based on the E2V equation) was found to fit very well for exposures of 30s:

$$I_{\rm dark} = 1.6 \times 10^9 \times T^3 \exp(-6400/T), \qquad (1)$$

where $I_{\rm dark}$ = dark current in e^- pix^{-1} hour^{-1} and T = temperature in degrees Kelvin. This model is shown overlaid on the measured data points in Figure 1. Note that this equation holds specifically for 30s exposures. For reasons explained in Section 4, the dark current (i.e. charge per unit time) is not necessarily constant with exposure time.

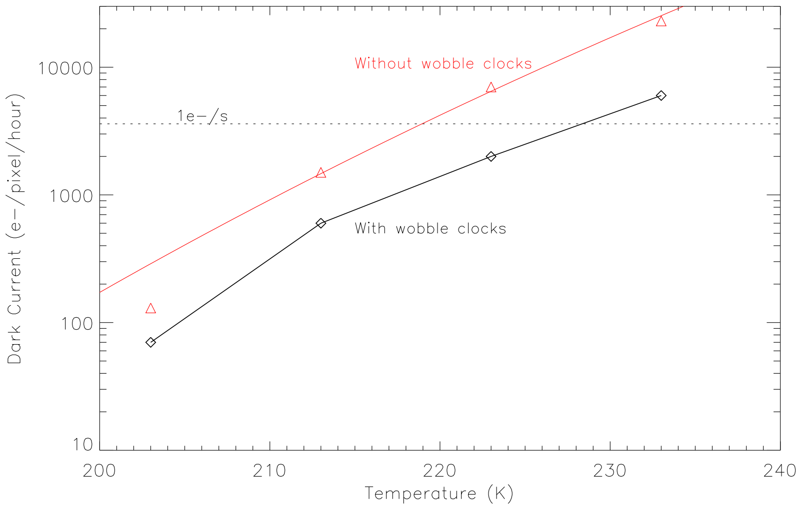

Figure 1: Dark current as a function of temperature for exposure times of 30s both with an without wobble clocking. Wobble clocking was done at a frequency of 100Hz. The continuous red line is based on the manufacturers dark current model.

4 Use of 'wobble-clocking'

Dark current has two main components : surface and bulk. The bulk component can only be reduced by cooling. At the surface of the CCD below the Si0_2 insulating layer that separates the electrodes from the underlying Silicon the surface component is generated. Here there are mid-band interface states that allow an easier path for thermally generated electrons to reach the conduction band and appear as photo-charge. This surface component can be about 2 orders of magnitude higher than the bulk component. Its effect can be reduced greatly by holding the vertical phases in their inverted (low) states. This injects holes into the surface of the CCD where they have a lifetime exceeding an hour at typical LN_2 operating temperatures (Burke & Gajar [1]). At higher temperatures they can still have lifetimes of order of seconds. While they persist, these holes mop up any surface dark current. When a CCD is vertically clocked, for example during the clear operation prior to an exposure, each vertical clock becomes inverted at some point in the charge transfer process. This means that for a short time after a clear (or indeed after any vertical phase modulation that creates inversion) the dark current of a CCD is temporarily suppressed. The effect is very obvious when operating at Peltier temperatures (>200K). At cryogenic temperatures (<180K) the effect is not so noticeable since the dark current is already very low and the hole lifetime much greater than typical exposure times.

It is also possible to invert the vertical phases of the CCD42C0 during integration in order to suppress the surface dark current. This has to be done in a sequential manner so that at least one phase is held high at any one time. It is also necessary to keep each pixel charge packet within the same pixel during integration or the image may become smeared. This was achieved by modulating the vertical phases with the sequence shown in Table 1. The total duration of this sequence was 300μs. Modulating the vertical phases is known as ‘wobble-clocking’ or ‘dither-clocking’.

As an experiment, this sequence of vertical clock transitions was applied to the CCD42CO every 10ms throughout a 30s exposure and the dark current measured. The result is plotted as the black line in Figure 1. As can be seen the effect was very pronounced and the dark current was suppressed by a factor of approximately four.

In the next experiment a series of 30s exposures was taken at various temperatures and various wobble clock frequencies. Initially the wobble clock sequence shown in Table 1 was applied to the vertical phases every 1ms during the course of the

Table 1: Wobble clocking sequence. The table shows the sequence of clock voltages applied to the vertical phases. H=+3V, LO=-9V with respect to substrate.

Vϕ1	Vϕ2	Vϕ3
LO	HI	LO
HI	HI	LO
HI	LO	LO
HI	HI	LO
LO	HI	LO
LO	HI	HI
LO	LO	HI
LO	HI	HI
LO	HI	LO

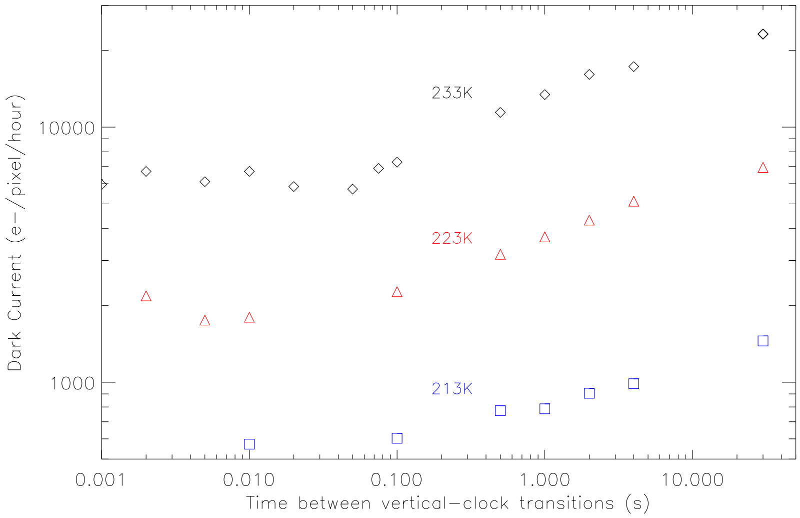

Figure 2: Dark current suppression using wobble clocking at various frequencies and temperatures.

dark exposure. The period between 'wobbles' was then slowly increased up to the maximum of 4s that was allowed by the controller. At each of these periods another 30s dark frame was taken. Finally the wobble clocks were disabled and a simple 30s dark frame with constant clock voltages was taken. The measured dark currents are shown plotted for 3 different temperatures in Figure 2. Note that the plot corresponding to 233K shows a steady decline in dark current as the wobble period decreases to approximately 50ms. At shorter periods the dark current then levels off. At 223K the dark current levels off at about 200ms. This longer period is expected since the hole lifetime is greater at lower temperatures. The graph also shows plotted the non-wobble 30s dark frames. The vertical clock phases were constant during these exposures but one must remember that immediately prior to the exposure a clear operation inverted in sequence all the vertical phases and so injected dark-current suppressing holes in the same manner as a wobble clock sequence. This graph then shows us approximately what wobble clock frequency we need to use to suppress the dark current efficiently at each temperature.

4.1 Wobble-clock induced cosmetic defects

The use of wobble clocking can produce a cosmetic effect known as pocket pumping (Janesick [3]). If the CCD contains charge traps then the repeated passage of a charge packet through the trap zone can cause a multiplication in the amount of charge in the trap. The effect can cause bright spots to appear in flat field images.

To investigate pocket pumping the CCD was given a brief exposure by the LED mounted outside the cryostat window. After this exposure, but before the commencement of readout, the wobble clocks were then applied with a frequency of 1KHz (i.e. the sequence shown in Table 1 was repeated at intervals of 1ms) for a period of 10s. The frame was then read out and compared with another frame taken with no wobble clocks. The tests were done at a temperature of 220K and the LED exposure level was between a few thousand and 20kADU (the illumination was not uniform). The frames were then subtracted one from the other to produce a 'difference frame' that revealed the cosmetic defects introduced by the wobble clocks. One complication to this technique was the contamination from cosmic ray events. To overcome this, a total of 5 frames were taken with and without wobble clocks. Each group of 5 frames was then averaged, discarding the maximum and minimum pixel values at each location.

A small section of the difference frame is shown in Figure 3. Three defects can clearly be seen. Note that they appear as a bright pixel lying 1 row above a dark pixel. They had an approximate density of 1 defect pair per every 14000 pixels.

Six defects were randomly selected from the difference frame and vertical cuts made through each. These are shown in Figure 4. Note that the defects appear to conserve charge; the signal subtracted from the lower pixel appears added to the upper pixel.

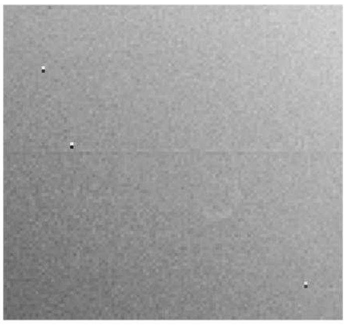

Figure 3: Wobble clock induced cosmetic defects in a small section of an image.

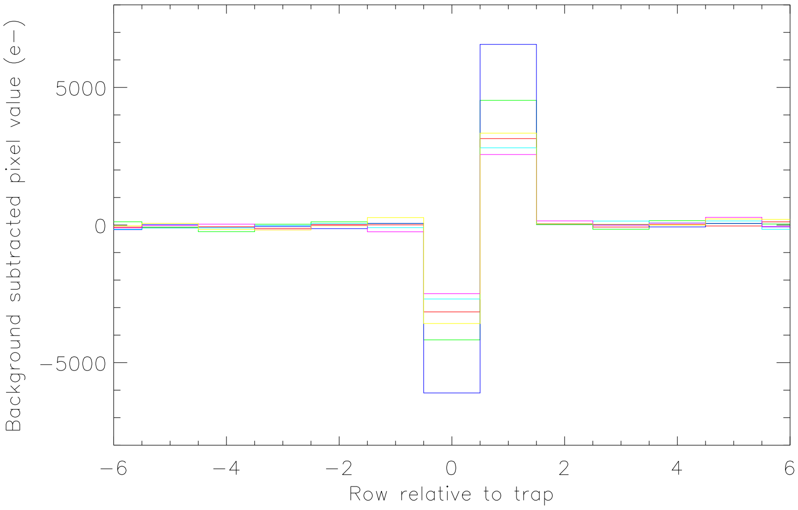

Figure 4: Column profiles through six randomly selected wobble-clock induced cosmetic defects. The image had been subjected to 10000 wobble clock transitions after exposure but before readout.

The measurements were then repeated with lower wobble clock frequencies. Figure 5 shows that the defects are lower in amplitude and therefore approximately proportional to the total number of wobble clock cycles. In this case each cycle appeared to add between 0.25 and 1.5 e^-. A CCD operated at 233K requires wobble clocks with a frequency of about 10Hz (see Figure 2). A 10s exposure may therefore see typical defect amplitudes of up to $150e^-$.

The majority of the defects had the same form: a bright pixel lying above a dark pixel. As an experiment the wobble clock sequence was reversed to see if it changed this orientation. The results are shown in Figure 6. As can be seen the only effect was to slightly reduce the amplitude of the defects (by about 30%).

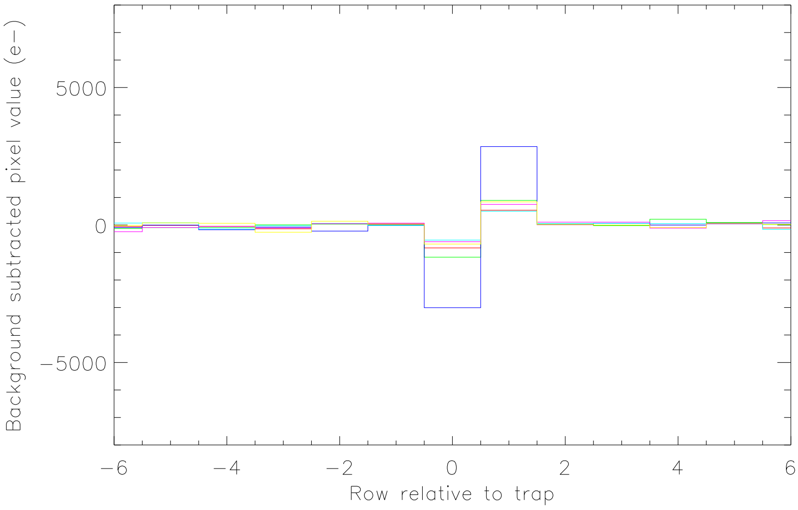

Figure 5: Column profiles through six randomly selected wobble-clock induced cosmetic defects. The image had been subjected to 2000 wobble clock transitions after exposure but before readout.

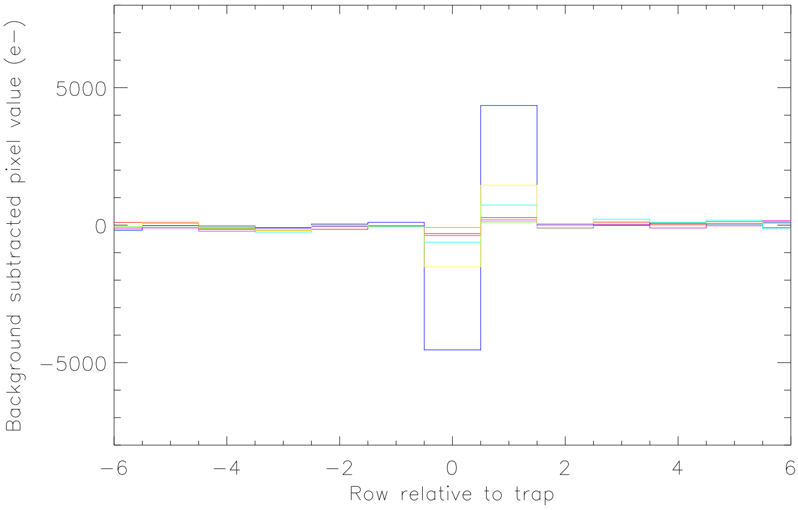

Figure 6: Column profiles through six randomly selected wobble-clock induced cosmetic defects. The image had been subjected to 10000 wobble clock transitions after exposure but before readout. The sequence of clock transitions was reversed compared to those used to generate the images analysed in Figure 4.

5 Dark current cosmetics

Operating at elevated temperatures can cause dark current non-uniformities producing considerable structure to appear in the dark frames. This is shown in Figure 7. Since dark current may change with exposure time it is essential that a series of dark frames be taken with the same exposure times as the science frames.

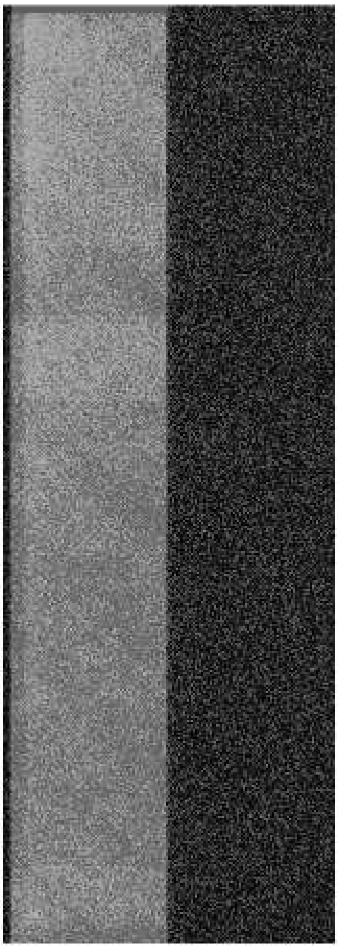

Figure 7: Dark current non-uniformity. The image shows a 30s dark frame taken at 233K. The right hand of the CCD was not working so shows just a bias level.

6 Conclusion

The Eddington CCD needs to be operated at <220K if dark currents below 1e^{-}s^{-1} are to be achieved. Wobble clocking will give the same dark current performance at approximately 230K but will introduce cosmetic defects due to the phenomenon of pocket pumping. For the CCD used in these tests the number of defects was approximately 1 in every 120x120 pixel window. The defects conserved charge so although they cause a distortion of the image they do not affect photometry.

References

[1] Burke B. E., Gajar S. A., 1991, IEEE Transactions on Electron Devices, 38, 285

[2] Jorden P. R., Pool P., Tulloch S. M., 2004, in Amico P., Beletic J. W., Belectic J. E., eds, Scientific Detectors for Astronomy, The Beginning of a New Era Vol. 300 of Astrophysics and Space Science Library, Secrets of E2V Technologies CCDs. pp 115–122

[3] Janesick J. R., 2001, Scientific Charge-Coupled Devices. SPIE Press, PO Box 10, Bellingham,WA